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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,540	08/28/2000	Alexander D. Schapira	246/214	7789

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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,540	SCHAPIRA ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No: _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment filed July 25, 2006. Claims 1 - 18 are pending. Claims 1 - 18 have been examined. Claims 1 - 18 have been rejected. Claims 1 - 18 are allowable over the prior art of record.

2. **The Examiner would like to thank the Applicant for the well-presented response, which was useful in the examination process. The Examiner would also like to thank the Applicant for calling the Examiner to resolve the issues in the previous Office Action, thereby expediting the examination process.**

3. This Office Action is NON-final because of new rejections made under 35 USC § 101.

Response to Remarks

4. Regarding claim 12 objected to for minor informalities:
   a. Applicant's amendment overcomes the objection.

5. Regarding **claims 3 - 7, 9 - 12 and 18** rejected under 35 USC § 112:
   a. Applicant's arguments (see pages 9 - 11) have been fully considered and are persuasive. Therefore, the rejections of the claims have been withdrawn. Regarding claim 18, after further consideration, the rejection is withdrawn.

6. Regarding objections to the drawings:
   a. Applicant submitted new drawings that overcome the objection.

7. Regarding objection to the specification:
   a. Applicant's argument overcomes the objection.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. **Claims 1 - 18** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding **claims 1 - 18**, the claims do not appear to produce a useful and tangible result to form the basis of a practical application needed to be statutory. The claims appear to perform calculations, simulations and determinations, but do not appear to provide a clear useful and tangible result. Please note that computer hardware that does not provide a useful and tangible result is rejected under 35 USC § 101.

Allowable Subject Matter

10. Claims 1 - 18 are allowable over the prior art of record.

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

12. A reasons for indicating allowability of claims 1, 8, 13, 14 and 17 was provided in the previous Office Action.

13. The following is a statement of the Examiner's reasons

14. Regarding claim 3, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "a node at which said digital circuit provides an output and at which said analog circuit receives an input, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state; modeling said output as a digital output signal from said digital circuit to said node when said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output is in said high impedance state; and dynamically switching between said digital output signal and said analog output signal based upon whether or not said output is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

15. Regarding claim 5, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "said interface comprising a node at which each of said plurality of digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state,

digital low state, or a high impedance state; modeling at least one of said outputs as a digital output signal from the corresponding digital circuit to said node when said at least one output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one output is in said high impedance state; and dynamically switching between said digital output signal and said analog output signal based upon whether or not said at least one output is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

16. Regarding claim 9, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state; and modeling at least one of said one or more outputs as a digital output signal from the corresponding digital circuit to said node when said at least one output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one output is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

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